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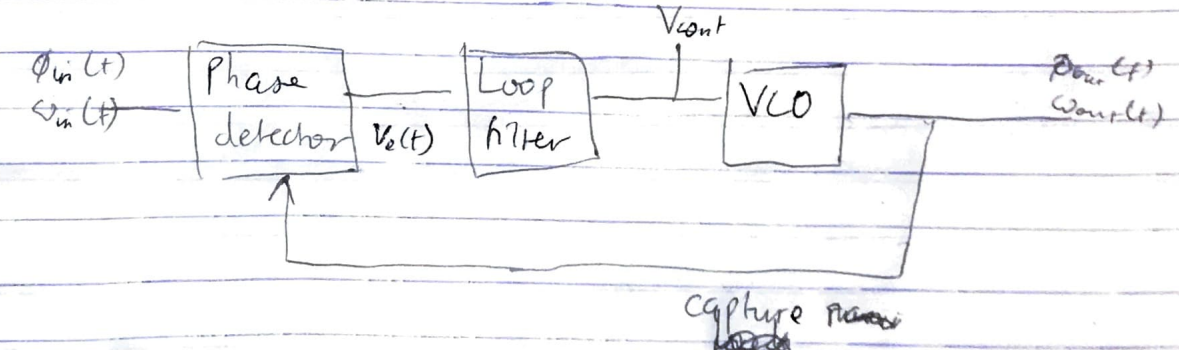
15/ENG04/025.
EEE 524

Analog ~~Multipliers~~.
PLL Circuits.

Applications of PLL.
(a) Clock generation.
(b) Frequency synthesizers.
(c) Clock recovery in a serial data link.

Phase locked loop is a control system or control loop which maintains the same phase between the input and output signal.

PLL Block.



capture range

- Whenever the input is in the capture range, the VCO can lock to the input signal.
- The lock range is a range of input signal frequencies over which the loop remains locked once it has captured the signal.
- The capture range is the range of input frequencies around the VCO onto which the loop will lock when starting from an unlocked condition

- The phase detector in an RF ~~sys~~ application is a balanced mixer while in digital signal is a XOR gate.

The diagram

When output is taken from the V_{out} terminals a base output is produced that traces the variation in phase of the input

When output is taken from the VCO, it acts as an oscillator to generate clock signals that digital systems utilize to function.

Relationship between phase and frequency.

$$\omega(t) = \frac{d\phi}{dt}$$

$$\phi(t) = \phi(0) + \int_0^t \omega(t)\, dt.$$

where ϕ = phase.

ω = frequency.

Jotter.

PNP NPN

Analog multipliers.

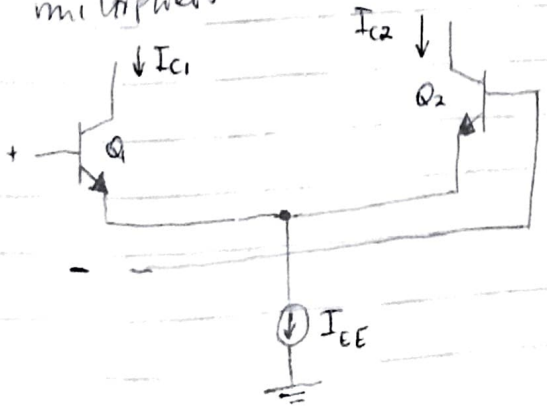
These operations include.
- rectification
- modulation
- demodulation
- frequency translation
- multiplication
- division

- We are going to analyze two of the most common operations in a monolithic IC (Division and multiplication).

- Often in analog-signal processing a need arises for when 2 analog inputs are multiplied and a proportional output is given.

- Such circuits are known as analog multipliers.
- We are going to examine several analog multipliers that depend on the exponential transfer function of bipolar transistors.

The emitter coupled pair as a simple multiplier.



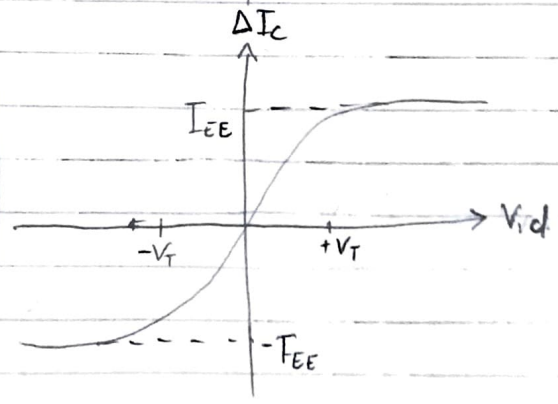
- output currents I_{C1} and I_{C2} were produced in relation to a differential input voltage V_{id}.

$$I_{C1} = \frac{I_{EE}}{1+\exp(-V_{id}/V_T)}$$

$$I_{C2} = \frac{I_{EE}}{1+\exp(V_{id}/V_T)}$$

$$\Delta I_C = I_{C1} - I_{C2}.$$
$$= I_{EE} \tanh(V_{id}/2V_T)$$

- The relationship is plotted and it shows the emitter-coupled pair can be used as a primitive multiplier.



or assuming $(V_{id}/2V_T) << 1$
$\Rightarrow I_{EE} \Delta I_C = I_{EE}(V_{id}/2V_T)$

- I_{EE} is the bias current for the emitter couple pair.
- If we add more circuitry we can make I_{EE} proportional to a second input signal.
- Thus $I_{EE} \cong k_0(V_{i2} - V_{BE(on)})$.
- Differential output current.

$$\Delta I_C \cong k_0 V_{id}(V_{i2} - V_{BE(on)})/2V_T$$

as a multiplier.

- This is a circuit that functions under the assumption that V_{id} is small and that V_{i2} is greater than $V_{BE(on)}$
- This multiplier can only function in 2 quadrants of the $V_{id} - V_{i2}$ plane and is called a 2 quadrant multiplier.
- The Gilbert multiplier cell is a modification and allows 4 quadrant multiplications